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Schneegans et al.

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(54) **SEMICONDUCTOR DEVICE COMPRISING A PROTECTIVE STRUCTURE ON A CHIP BACKSIDE AND METHOD OF PRODUCING THE SAME**

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(22) Filed: **Dec. 14, 2012**

(65) **Prior Publication Data**

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(51) **Int. Cl.**

H01L 21/00	(2006.01)
H01L 21/78	(2006.01)
H01L 29/45	(2006.01)
H01L 23/367	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 21/78*** (2013.01); ***H01L 23/3677*** (2013.01); ***H01L 29/45*** (2013.01); *H01L 2224/83191* (2013.01); *H01L 2924/1305* (2013.01); *H01L 2924/13055* (2013.01); *H01L 2924/13062* (2013.01); *H01L 2924/13091* (2013.01); *H01L 2924/1461* (2013.01)

(58) **Field of Classification Search**

CPC H01L 2224/03019; H01L 2224/94; H01L 24/94; H01L 24/93; H01L 24/80; H01L 24/27; H01L 24/29

USPC 438/114, 458, 459, 460, 462, 464, 465, 438/612, 780, 113, 613, 614, 666; 257/778, 257/779, 782, 783, 786, 619, 620, 618, 622

See application file for complete search history.

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(57) **ABSTRACT**

A semiconductor device includes a semiconductor chip including a first main face and a second main face. The second main face is the backside of the semiconductor chip. The second main face includes a first region and a second region. The second region is a peripheral region of the second main face and the level of the first region and the level of the second region are different. The first region may be filled with metal and may be planarized to the same level as the second region.

33 Claims, 9 Drawing Sheets

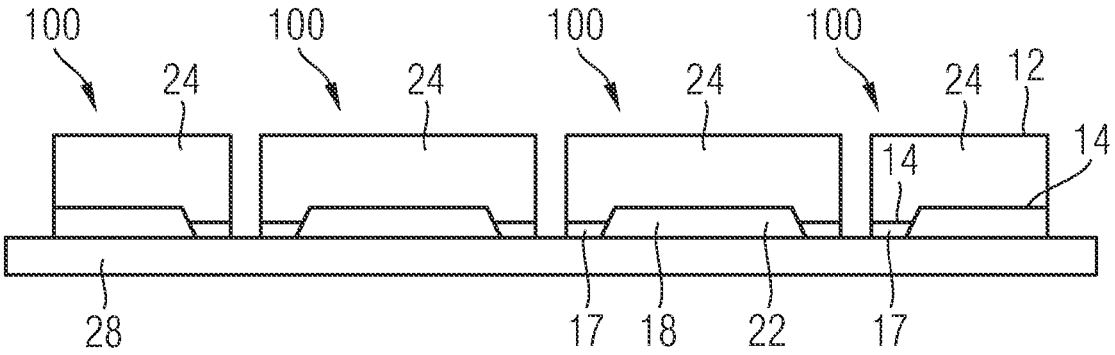


FIG 1A

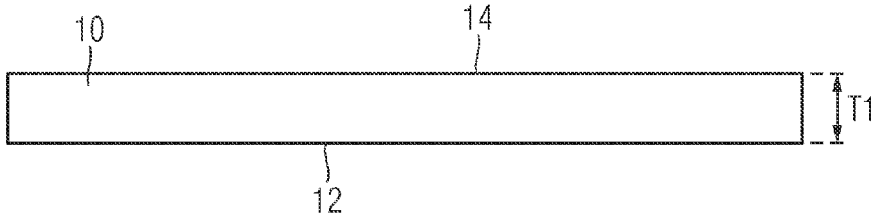


FIG 1B

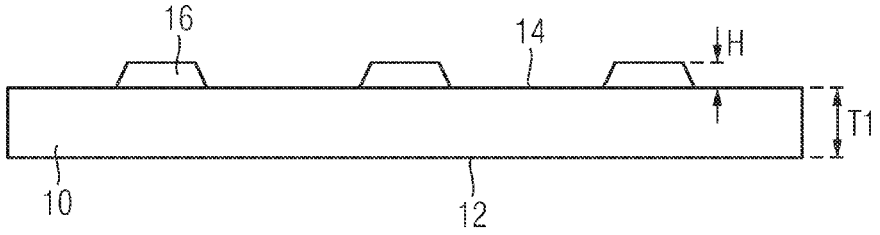


FIG 1C

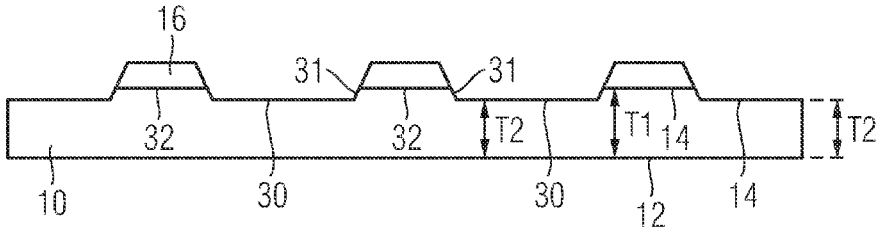


FIG 1D

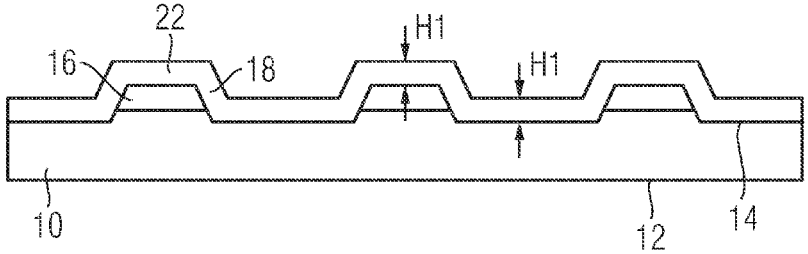


FIG 1E

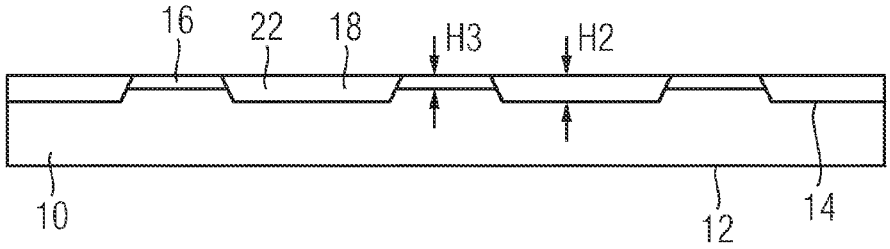


FIG 1F

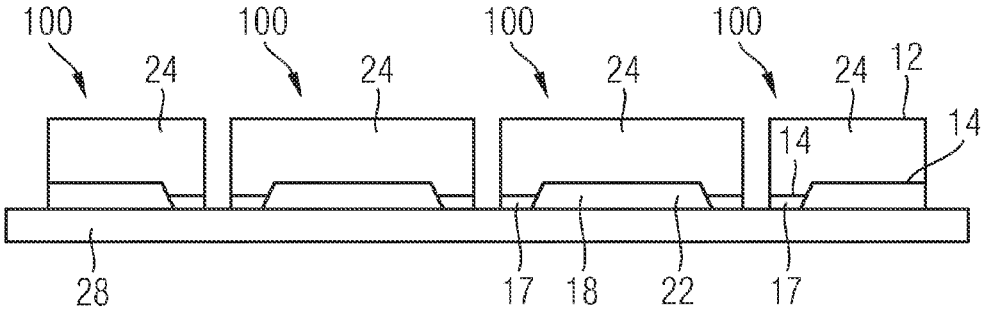


FIG 2A

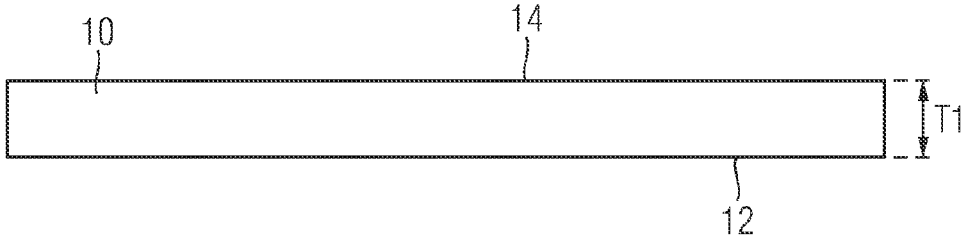


FIG 2B

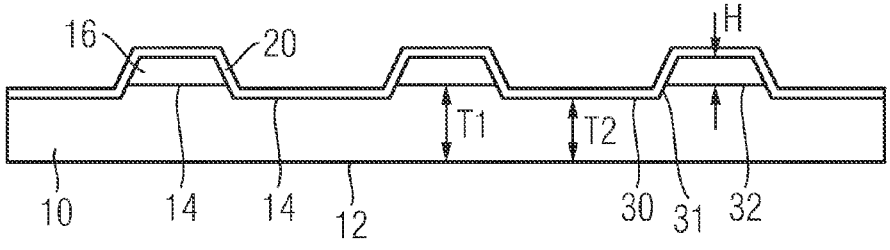


FIG 2C

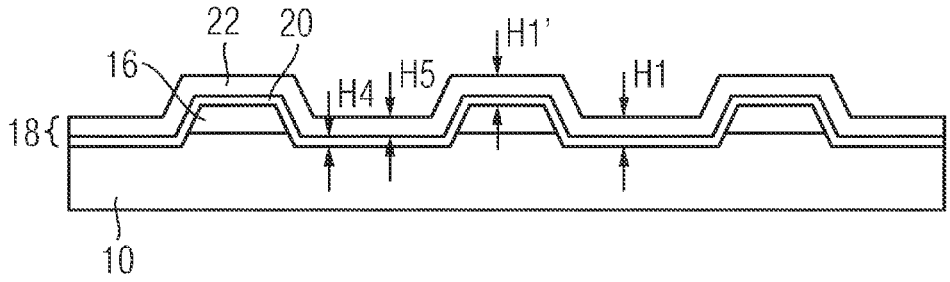


FIG 2D

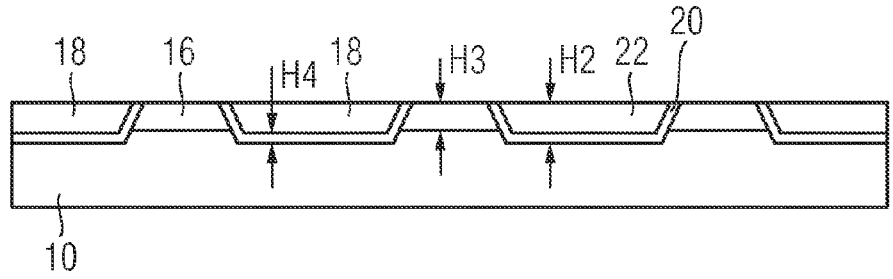


FIG 2E

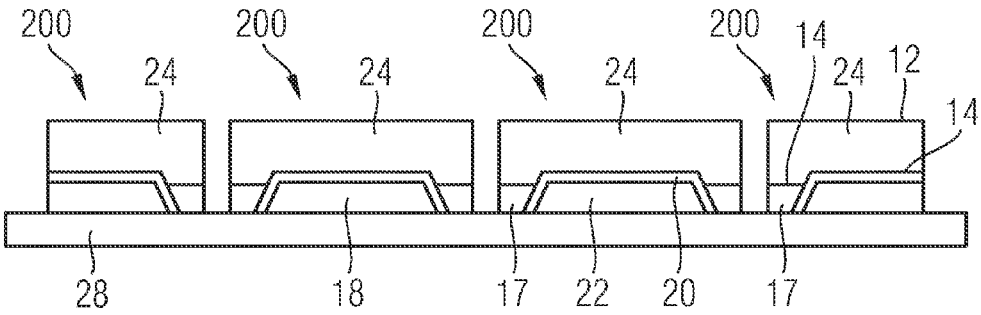


FIG 3A

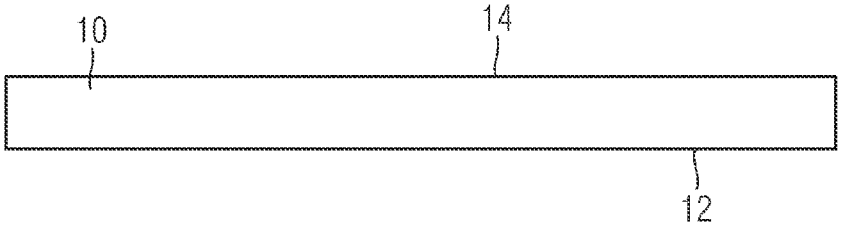


FIG 3B

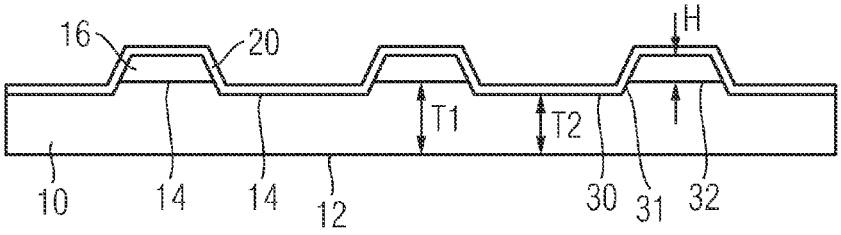


FIG 3C

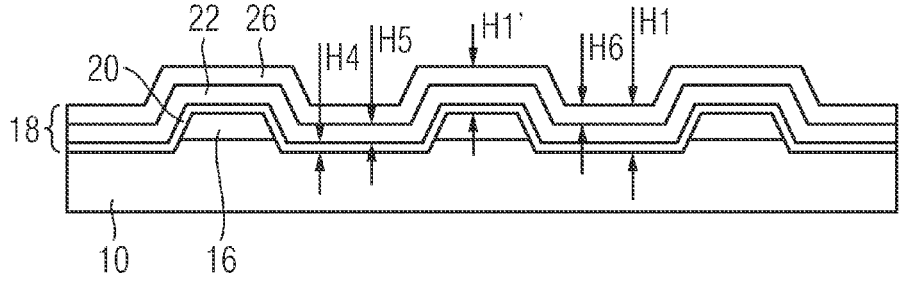


FIG 3D

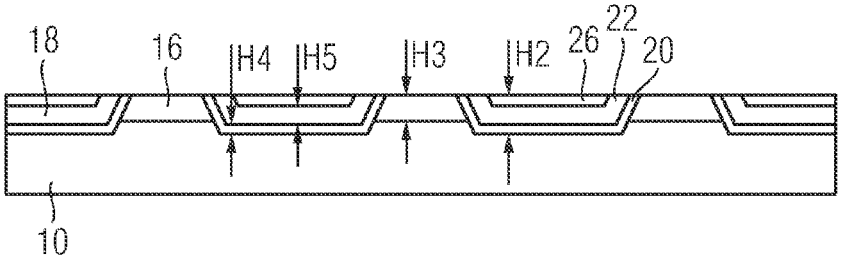


FIG 3E

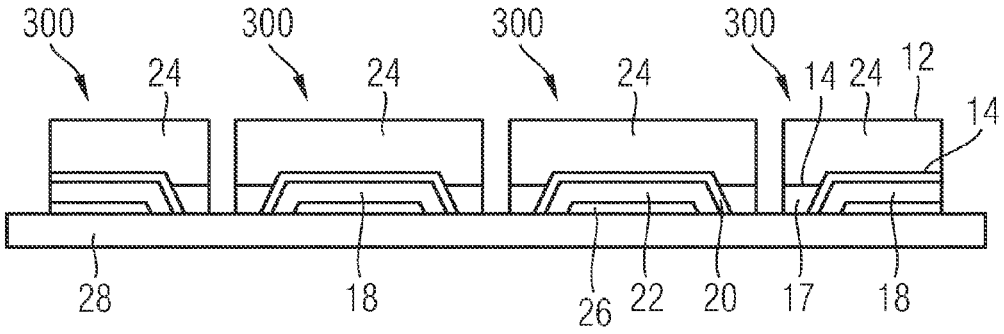


FIG 4A

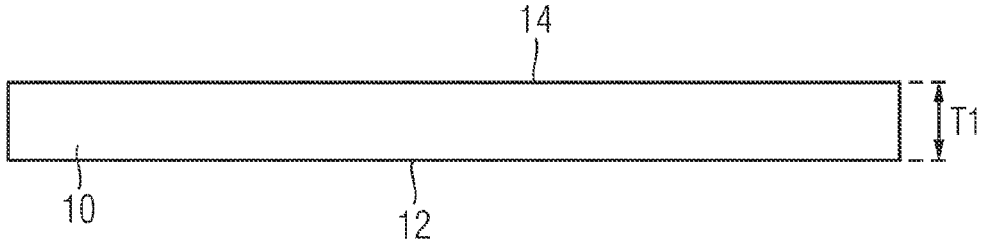


FIG 4B

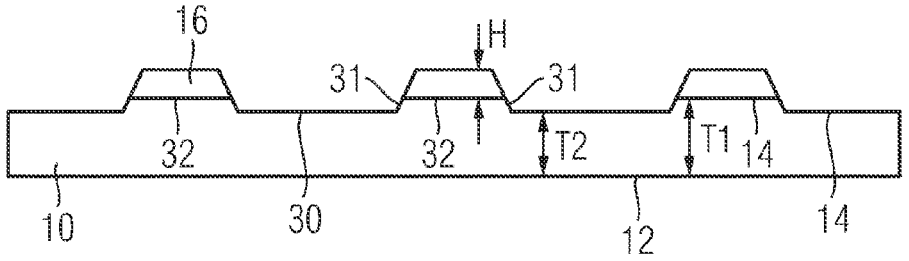


FIG 4C

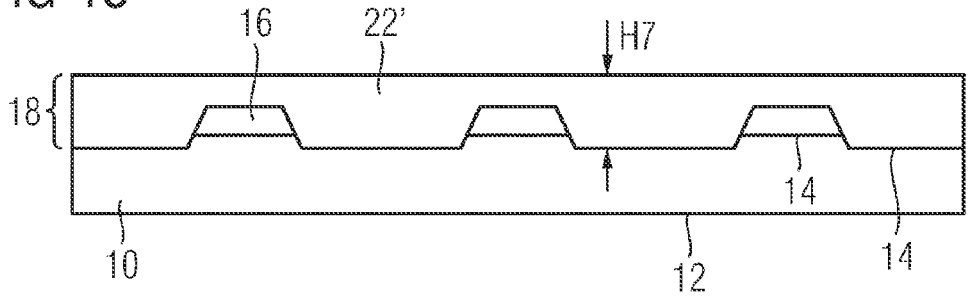


FIG 4D

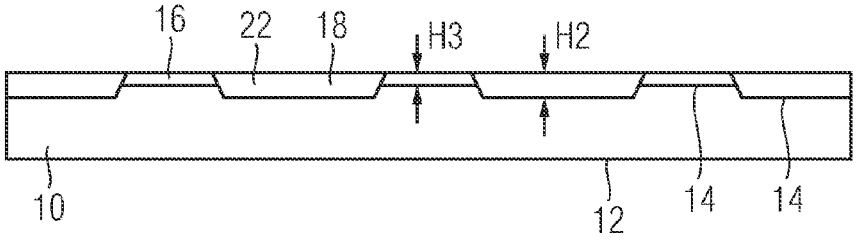


FIG 4E

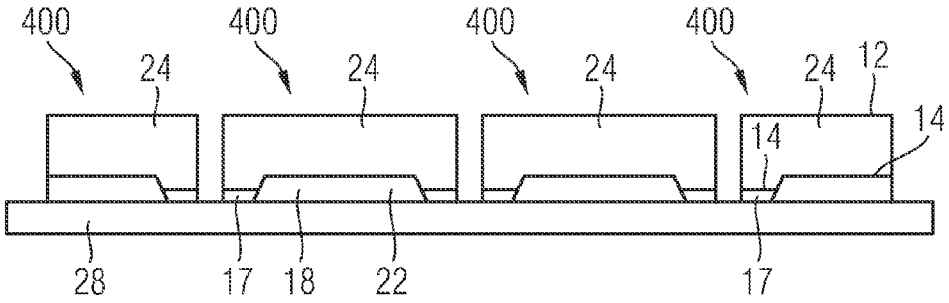


FIG 5A

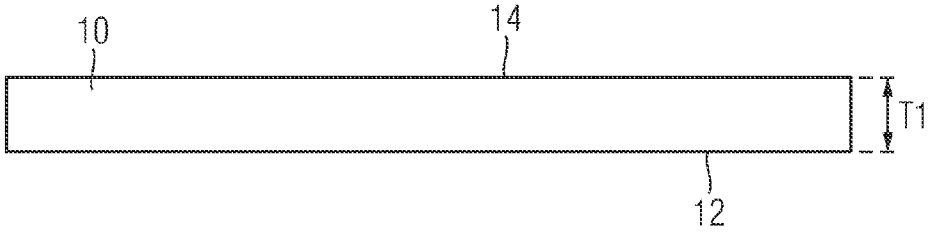


FIG 5B

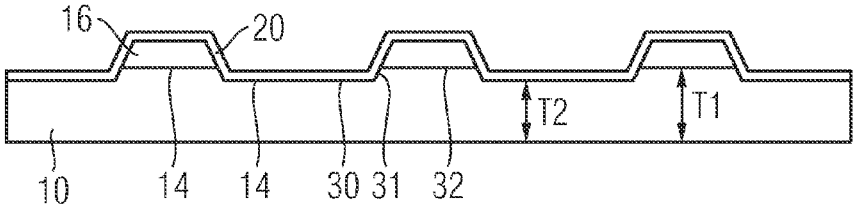


FIG 5C

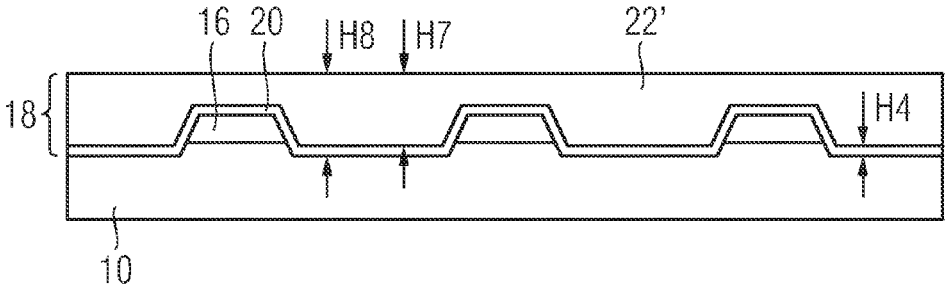


FIG 5D

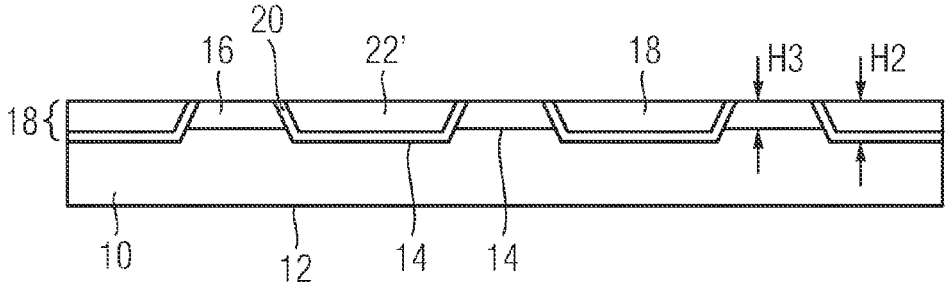


FIG 5E

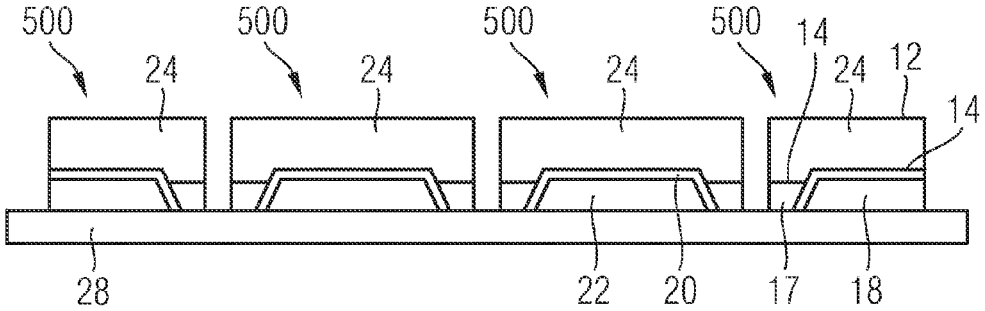


FIG 6

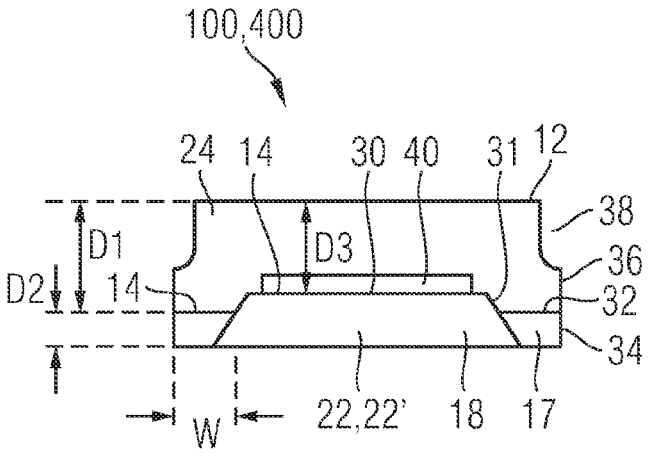


FIG 7

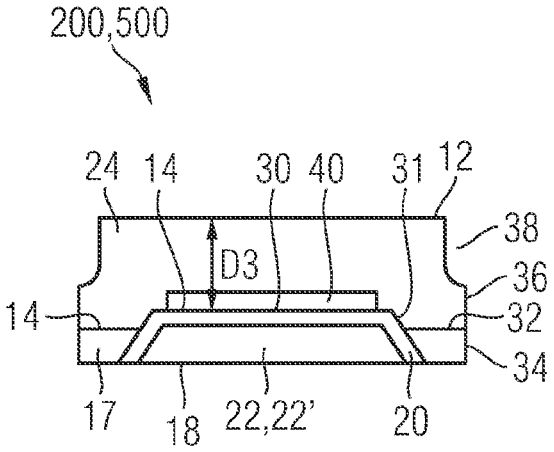


FIG 8

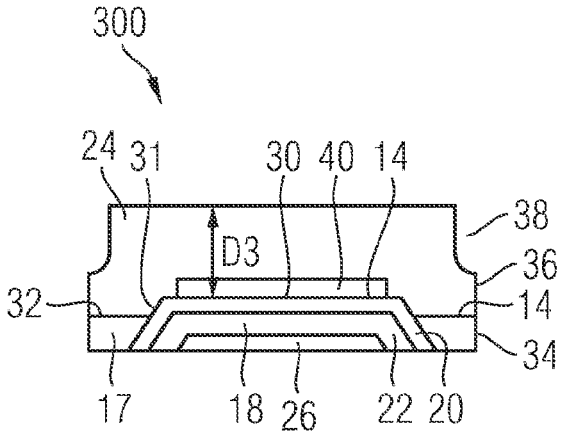


FIG 9

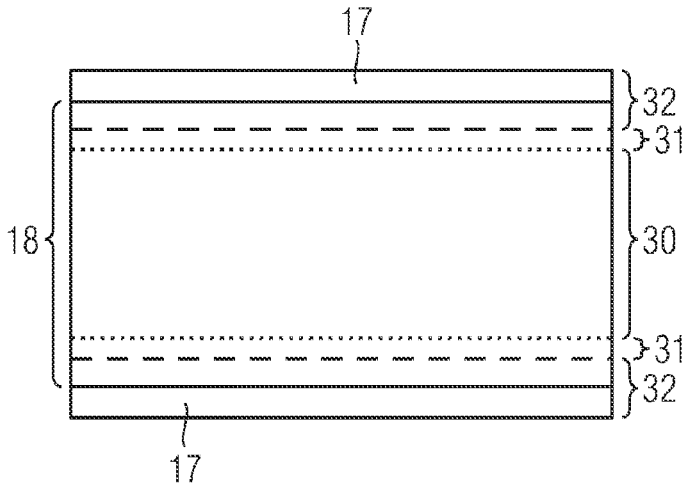


FIG 10

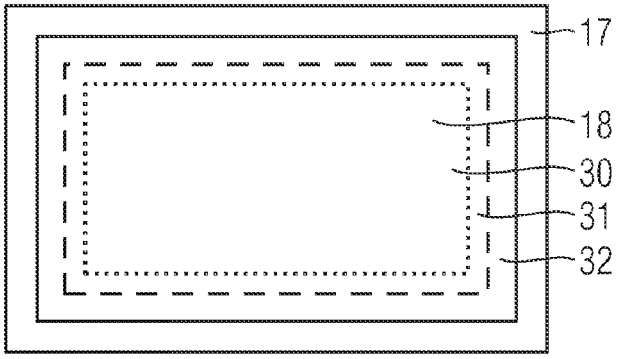
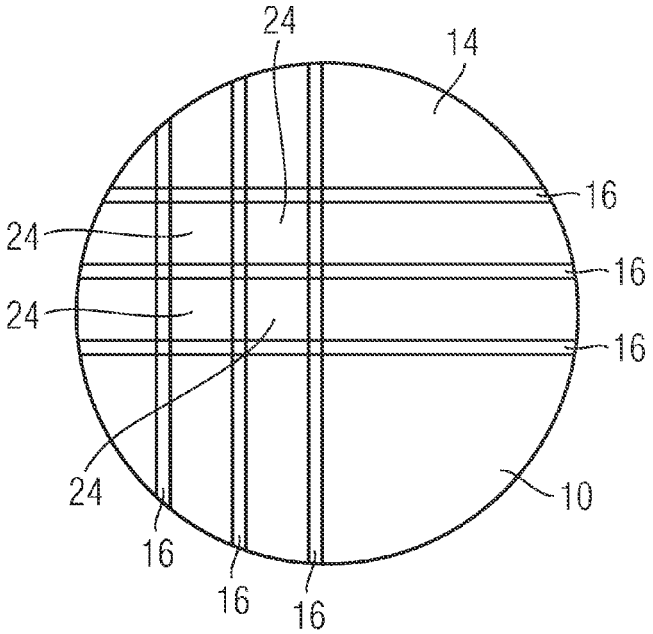


FIG 11



SEMICONDUCTOR DEVICE COMPRISING A PROTECTIVE STRUCTURE ON A CHIP BACKSIDE AND METHOD OF PRODUCING THE SAME

TECHNICAL FIELD

The invention relates to a semiconductor device and a method of manufacturing the same, and, in more particular embodiments, to the technology of separating a semiconductor substrate such as, e.g., a wafer into semiconductor units such as, e.g., chips. The invention further relates to a semiconductor device which has improved heat dissipation characteristics.

BACKGROUND

Semiconductor device manufacturers are constantly striving to increase the performance of their products, while decreasing their cost of manufacture. A cost intensive area in the manufacture of semiconductor devices is packaging the semiconductor chips. As those skilled in the art are aware, integrated circuits are fabricated on wafers, which are then singulated to produce semiconductor chips. Subsequently, the semiconductor chips may be mounted on electrically conductive carriers, such as lead frames. Packaging methods providing high yield at low expenses are desirable.

For these and other reasons, there is a need for the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are included to provide a further understanding of embodiments and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments and together with the description serve to explain principles of embodiments. Other embodiments and many of the intended advantages of embodiments will be readily appreciated as they become better understood by reference to the following detailed description.

FIGS. **1**A-**1**F schematically illustrate cross-sectional views of one embodiment of a method of manufacturing a semiconductor device;

FIGS. **2**A-**2**E schematically illustrate cross-sectional views of one embodiment of a method of manufacturing a semiconductor device;

FIGS. **3**A-**3**E schematically illustrate cross-sectional views of one embodiment of a method of manufacturing a semiconductor device;

FIGS. **4**A-**4**E schematically illustrate cross-sectional views of one embodiment of a method of manufacturing a semiconductor device;

FIGS. **5**A-**5**E schematically illustrate cross-sectional views of one embodiment of a method of manufacturing a semiconductor device;

FIG. **6** schematically illustrates a cross-sectional view of one embodiment of a semiconductor device;

FIG. **7** schematically illustrates a cross-sectional view of one embodiment of a semiconductor device;

FIG. **8** schematically illustrates a cross-sectional view of one embodiment of a semiconductor device;

FIG. **9** schematically illustrates a bottom view of one embodiment of a semiconductor device;

FIG. **10** schematically illustrates a bottom view of one embodiment of a semiconductor device; and

FIG. **11** schematically illustrates a bottom view of a wafer having a structured backside conductive layer.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

Aspects and embodiments are now described with reference to the drawings, wherein like reference numerals are generally utilized to refer to like elements throughout. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of one or more aspects of the embodiments. It may be evident, however, to one skilled in the art that one or more aspects of the embodiments may be practiced with a lesser degree of the specific details. In other instances, known structures and elements are shown in schematic form in order to facilitate describing one or more aspects of the embodiments. The following description is therefore not to be taken in a limiting sense, and the scope is defined by the appended claims. It should also be noted that the representations of the various layers, sheets or substrates in the figures are not necessarily to scale.

In the following detailed description, reference is made to the accompanying drawings, which form a part thereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. In this regard, directional terminology, such as "top," "bottom," "front," "back," "leading," "trailing," etc., is used with reference to the orientation of the figure(s) being described. Because components of embodiments can be positioned in a number of different orientations, the directional terminology is used for purposes of illustration and is in no way limiting. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

It is to be understood that the features of the various exemplary embodiments described herein may be combined with each other, unless specifically noted otherwise.

As employed in this specification, the terms "coupled" and/or "electrically coupled" are not meant to mean that the elements must be directly coupled together; intervening elements may be provided between the "coupled" or "electrically coupled" elements.

The semiconductor chips described further below may be of different types, may be manufactured by different technologies and may include for example integrated electrical, electro-optical or electro-mechanical circuits and/or passives. The semiconductor chips may, for example, be configured as power semiconductor chips. Furthermore, the semiconductor chips may include control circuits, microprocessors or microelectromechanical components. Furthermore, the devices described below may include logic integrated circuits to control the integrated circuits of other semiconductor chips, for example the integrated circuits of power semiconductor chips. The semiconductor chips need not be manufactured from specific semiconductor material, for example Si, SiC, SiGe, GaAs, and, furthermore, may contain inorganic and/or organic materials that are not semiconductors, such as for example insulators, plastics or metals.

Semiconductor devices containing such semiconductor chips are described below. In particular, semiconductor chips having a vertical structure may be involved, that is to say that the semiconductor chips may be fabricated in such a way that electric currents can flow in a direction perpendicular to the

main faces of the semiconductor chips. A semiconductor chip having a vertical structure has electrodes on its two main faces, that is to say on its top side and bottom side (the bottom side is also referred to as backside herein).

In particular, the semiconductor device may include a power semiconductor chip. Power semiconductor chips may have a vertical structure. The vertical power semiconductor chips may, for example, be configured as power MOSFETs (Metal Oxide Semiconductor Field Effect Transistors), IGBTs (Insulated Gate Bipolar Transistors), JFETs (Junction Gate Field Effect Transistors), power bipolar transistors or power diodes. By way of example, the source electrode and gate electrode of a power MOSFET may be situated on one main face, while the drain electrode of the power MOSFET is arranged on the other main face.

The semiconductor chips may have contact pads (or electrodes) which allow electrical contact to be made with the integrated circuits included in the semiconductor chips. The electrodes may include one or more electrode metal layers which are applied to the semiconductor material of the semiconductor chips. The electrode metal layers may be manufactured with any desired geometric shape and any desired material composition. The electrode metal layers may, for example, be in the form of a layer covering an area. Any desired metal, for example Cu, Ni, Sn, Au, Ag, Pt, Pd, and an alloy of one or more of these metals may be used as the material. The electrode metal layer(s) need not be homogenous or manufactured from just one material, that is to say various compositions and concentrations of the materials contained in the electrode metal layer(s) are possible.

In several embodiments one or more conductive layers, in particular electrically conductive layers, are applied. It should be appreciated that any such terms as "formed" or "applied" are meant to cover literally all kinds and techniques of applying layers. In particular, they are meant to cover techniques in which layers are applied at once as a whole like, for example, laminating techniques as well as techniques in which layers are deposited in a sequential manner like, for example, sputtering, plating, molding, CVD (Chemical Vapor Deposition), PVD (physical vapor deposition), evaporation, hybrid physical-chemical vapor deposition (HPCVD), etc.

The applied conductive layer may comprise, inter alia, one or more of a layer of metal such as Cu or Sn or an alloy thereof, a layer of a conductive paste and a layer of a bond material. The layer of a metal may be a homogeneous layer. The conductive paste may containing metal particles distributed in a vaporizable or curable polymer material, wherein the paste may be fluid, viscous or waxy. The bond material may be applied to electrically and mechanically connect the semiconductor chip, e.g., to a carrier or, e.g., to a contact clip. A soft solder material or, in particular, a solder material capable of forming diffusion solder bonds may be used, for example solder material comprising one or more of Sn, SnAg, SnAu, SnCu, In, InAg, InCu and InAu.

A dicing process may be used to divide the wafer into individual chips. Any technique for dicing may be applied, e.g., blade dicing (sawing), laser dicing, etching, etc. In particular, stealth dicing, which is a specific technique using laser dicing may be applied. Stealth dicing allows suppressing cutting waste and is therefore a suitable process for cutting work pieces that are vulnerable to contamination. Further, it is a dry process that does not require cleaning, and is therefore also suitable for processing sensitive structures such as, e.g., MEMS, that are vulnerable to load. Further benefits which may be achieved by the stealth dicing technology are high-speed dicing, superior breakage strength, small kerf and low running costs.

In stealth dicing technology, a laser beam of a wavelength capable of transmitting through the semiconductor wafer is focused onto a point inside the semiconductor wafer. Due to a non-linear absorption effect, only localized points inside the semiconductor wafer may be selectively laser-machined, whereby damaging of the front and back surface of the semiconductor wafer may be avoided. The semiconductor wafer can be diced by moving the relative positions of the laser beam and the semiconductor wafer in order to scan the semiconductor wafer according to the desired dicing pattern.

The semiconductor wafer may be diced by applying the semiconductor wafer on a tape, in particular a dicing tape, apply the dicing pattern, in particular a rectangular pattern, to the semiconductor wafer, e.g., according to one or more of the above mentioned techniques, and pull the tape, e.g., along four orthogonal directions in the plane of the tape. By pulling the tape, the semiconductor wafer gets divided into a plurality of semiconductor dies (chips).

FIGS. **1**A-**1**F schematically illustrate a method of manufacturing a semiconductor device **100** in accordance with one embodiment. FIG. **1**A schematically illustrates providing a semiconductor wafer **10** having a first main face **12** and a second main face **14** wherein the second main face **14** is the backside of the semiconductor wafer **10**. In FIG. **1**A the backside of the semiconductor wafer **10** is depicted as the upper main face of the semiconductor wafer **10**. The semiconductor wafer **10** may, e.g., have a thickness T**1**. The semiconductor wafer **10** may, e.g., be disc-shaped having a rounded outline and the diameter of the semiconductor wafer **10** may, e.g., be equal to or greater than 200 or 300 mm.

A process called dicing before grinding (DBG) may have been applied to the semiconductor wafer **10** in the previous steps (not shown in FIGS. **1**A-**1**E). In the DBG process grooves are machined into the first main face **12** of the semiconductor wafer **10**. The grooves have a depth which is smaller than the thickness of the semiconductor wafer **10**, in particular 10 to 20 μm. The grooves may, e.g., run on the first main face **12** of the semiconductor wafer **10** in a region where the semiconductor wafer **10** has not been processed. The grooves may run along the dicing streets where the semiconductor wafer **10** will be cut to be singulated into at least one semiconductor chip **24**, as shown in FIG. **1**F.

The semiconductor wafer **10** as shown in FIG. **1**A may have been thinned in a previous step (not shown in FIGS. **1**A-**1**F). The step of thinning the semiconductor wafer **10** may, e.g., be performed after the DBG step. The thinned surface may, e.g., be the second main face **14** (backside) of the semiconductor wafer **10**.

The front side of the semiconductor wafer **10** may have been processed during front-end wafer processing to produce active structures such as, e.g., integrated circuits, pn junctions, transistors, micro-mechanical structures, etc. Processing the front side may be carried out before or after thinning the backside of the semiconductor wafer **10**. It is also possible that the thinned surface may, e.g., be the first main face **12** of the semiconductor wafer **10**. In this case the front side of the wafer **10** is thinned first, then the front side is processed to generate the active structures and, optionally, the grooves are machined into the front side. Thinning the semiconductor wafer **10** may comprise at least one of mechanical thinning, in particular grinding, chemical mechanical polishing (CMP), and wet etching. Thinning the semiconductor wafer **10** may also comprise all of the aforementioned processes. Thinning may, e.g., comprise mechanical thinning and a subsequent damage etching process. The entire main surface of the semiconductor wafer may be subjected to thinning.

After the two (optional) steps of DBG grinding and thinning, the semiconductor wafer **10** may, e.g., have a thickness T**1** smaller than 100 μm, in particular smaller than 60 μm, and more in particular smaller than 40 μm or even 30 μm. After thinning, the depth of the grooves may, e.g., be between 15% and 70% of the thickness of the thinned semiconductor wafer **10**.

Referring to FIG. **1**B, a plurality of polymer stripes **16** is formed on the second main face **14** of the semiconductor wafer **10**. In FIG. **1**B, the plurality of polymer stripes **16** may be formed by applying a polymer on the second main face **14** (i.e., backside) of the semiconductor wafer **10** by, e.g., spin coating, prebaking the resist-coated wafer, lithographic patterning of the photoresist, and hard baking (curing) the photoresist. The polymer stripes **16** may, e.g., comprise an imide, in particular a photoimide, a photoresist, a thermosetting material or a thermoplastic material.

At least one of the plurality of polymer stripes **16** may, e.g., have a thickness or height H between 3 and 50 μm, in particular between 6 and 25 μm, more in particular between 9 and 15 μm. At least one of the plurality of polymer stripes **16** may, e.g., have a bottom width (at the second main face **14**) between 5 and 100 μm, in particular between 10 and 60 μm. A top width (at the exposed top face of the polymer stripes **16**) may, e.g., be identical or smaller than the bottom width.

The width of at least one of the plurality of polymer stripes **16** may, e.g., decrease from the second main face **14** in a direction away from the semiconductor wafer **10**. The polymer stripes **16** may, e.g., have a trapezoid or rectangular cross-section. The polymer stripes **16** may, e.g., be arranged equidistantly. The plurality of polymer stripes **16** may, e.g., be formed using at least one of lithography, in particular photolithography, printing, and dispensing.

The plurality of polymer stripes **16** may, e.g., be formed on the second main face **14** of the semiconductor wafer **10** at positions of the semiconductor wafer **10** opposite to the positions of the optionally formed grooves. In particular the spacing of the grooves may, e.g., be the same as the spacing of the plurality of polymer stripes **16**. The plurality of polymer stripes **16** may correspond to and overlay the dicing streets.

FIG. **1**C illustrates removing wafer material at the exposed portions of the second main face **14** of the semiconductor wafer **10**. By doing so, the semiconductor wafer **10** is selectively thinned in regions between the polymer stripes **16** on the second main face **14** of the semiconductor wafer **10** while the region of the second main face **14** of the semiconductor wafer **10** where the plurality of polymer stripes **16** is arranged remains unchanged. By removing wafer material at the exposed second main face **14**, the second main face **14** will obtain a surface which is structured in view of its level, i.e., is not flat. There may be first regions and second regions, wherein the level of the first regions and the level of the second regions are different. In the case of the embodiment of FIG. **1**C, after removing wafer material at the exposed first regions of second main face **14** of the semiconductor wafer **10**, the second main face **14** comprises first regions **30** having a distance T**2** from the first main face **12** and second regions **32** having a distance T**1** from the first main face **12**. The first regions **30** may essentially be flat. The same applies to the second regions **32**. Intermediate regions **31** may be arranged between each first region **30** and second region **32**. In the embodiment of FIG. **1**C, the distance of the intermediate region **31** to the first main face **12** rises from T**2** adjacent to the first region **30** to T**1** adjacent to the second region **32**. The intermediate region **31** may comprise the slope which connects the first region **30** with the second region **32**. The thickness T**2** of the semiconductor wafer **10** in the first region **30** may, e.g., be smaller than 50, 30, 20 or 15 μm. The difference in level between the first regions **30** and the second regions **32** may be greater than 3, 5, 10, 20 or 20 μm. The second regions **32** provide mechanical strength and rigidity to the semiconductor wafer **30** and finally also to diced chips, see FIGS. **6**-**8**. This allows to manufacture a semiconductor wafer **10** having a small thickness T**2** at the first regions **30** where the active structures are located.

Removing wafer material at the exposed second main face **14** of the semiconductor wafer **10** may, e.g., be performed by etching, in particular dry etching or wet etching. Dry etching may, e.g., be done using plasma etching. Other techniques for selective thinning are also feasible.

Depending on the used etching technique, the surface of the first region **30** of the second main face **14** of the semiconductor wafer **10** may be ablated evenly or unevenly. In particular the used etching may be isotropic or anisotropic. The slope of the surface of the intermediate region **31** may, e.g., be the same as the slope of the surface of at least one polymer stripe **16** adjacent to the intermediate region **31**. The plurality of polymer stripes **16** is not changed or influenced by the etching process.

FIG. **1**D illustrates forming a conductive layer **18** on the plurality of polymer stripes **16** and on the second main face **14** of the semiconductor wafer **10**. The conductive layer **18** may, e.g., be a first metallization layer **22**, i.e., a layer that comprises or consists of a first metal material. The first metal material may e.g. comprise or consist of one of Cu, Sn, and an alloy of one or more of these metals. The first metallization layer **22** may, e.g., be homogeneous. By way of example, the first metallization layer **22** of FIG. **1**C may be formed by sputtering a Cu and/or Sn material. However, as will be explained further below in conjunction with FIGS. **4**A-**4**E, the conductive layer **18** may also comprise or consist of a metal paste containing metal particles dispersed within an organic material, in particular a nano paste, a solder paste, in particular a diffusion solder paste, or a conductive adhesive.

Forming the conductive layer **18** (e.g., the first metallization layer **22**) on the plurality of polymer stripes **16** and on the second main face **14** of the semiconductor wafer **10** may, e.g., comprise at least one of sputtering, CVD, PVD, electroplating, electroless plating, and spray plating. As will be explained further below in conjunction with FIGS. **4**A-**4**E, the conductive layer **18** may, e.g., also be formed by at least one of squeegeeing, printing, dispensing, laminating, and spin-coating.

The thickness of the conductive layer **18** (e.g., first metallization layer **22**) may be H**1** in regions between adjacent polymer stripes **16**. The thickness of the conductive layer **18** on top of one of the plurality of polymer stripes **16** may be H**1'**. H**1** and H**1'** may, e.g., be about the same or may, e.g., be different. The thickness H of the plurality of polymer stripes **16** may, e.g., be greater than H**1**. Alternatively, the thickness H of the plurality of polymer stripes **16** may, e.g., be smaller than or equal to H**1**. H**1** may, e.g., be greater than 5, 10, 15, 20, 25, 30, 50 μm.

FIG. **1**E illustrates planarizing the conductive layer **18**. The conductive layer **18** (e.g., the first metallization layer **22**) may be planarized by using a mechanical planarization technique such as, e.g., at least one of grinding, milling, cutting, and chemical mechanical polishing (CMP). For planarizing the conductive layer **18** a surface planer may be used such as, e.g., the surface planer produced by the Japanese Disco Corporation, in the particular the surface planer DFS 8910 may, e.g., be used.

Both the conductive layer **18** and the plurality of polymer stripes **16** may, e.g., be planarized. In this case, as illustrated

in FIG. **1**E, the plurality of polymer stripes **16** is exposed. That is, the plurality of polymer stripes **16** is exposed at the surface of the semiconductor device **100** and the conductive layer **18** is transformed or structured into a plurality of separated stripes or lands, each of which is arranged between adjacent polymer stripes **16**.

FIG. **1**E illustrates that after planarization, the upper surface of the (structured) conductive layer **18** levels with the upper (exposed) surface of the plurality of polymer stripes **16**. Further, the lower surface of the conductive layer **18** may be lower than the lower surface of the plurality of polymer stripes **16**. A thickness H**2** of the (structured) conductive layer **18** may, e.g., be greater than a thickness H**3** of the plurality of polymer stripes **16**. It is to be noted that H**3** may be smaller than H, i.e., that the exposed surfaces of the polymer stripes **16** in FIG. **1**E are surfaces created by planarization. It is also to be noted that H**2** may be smaller than H**1**, i.e., that the conductive layer **18** in regions between adjacent polymer stripes **16** has been thinned by the planarization of FIG. **1**E.

The thickness H**2** of the conductive layer **18** may be greater than 1, 3, 10, 15, 20, 25 or 50 μm. In particular for power semiconductor chips a thickness H**2** of at least 10 μm or more may be desired. The exposed surfaces of the plurality of polymer stripes **16** and the upper surfaces of the structured conductive layer **18** may completely cover the second main face **14** of the semiconductor wafer **10**.

According to another possibility (not shown), after planarizing the conductive layer **18** may, e.g., still be continuous, more particularly may, e.g., still completely cover the semiconductor wafer **10**. In this case, there may be a thin residual layer of conductive material left on top of the plurality of the polymer stripes **16** and the plurality of polymer stripes **16** is not exposed. The thin residual layer of conductive material left on top of the plurality of the polymer stripes **16** may be as thin as not to overly impede the division process, i.e., may, e.g., be smaller than 5, 3 or 1 μm.

FIG. **1**F illustrates dividing the semiconductor wafer **10** into a plurality of semiconductor chips **24** or semiconductor devices **100**, e.g., by sawing, laser dicing or etching. To this end, the semiconductor wafer **10** may, e.g., be placed on a dicing tape **28** with the second main face **14** facing the dicing tape **28**, as shown in FIG. **1**F. The semiconductor wafer **10** may be divided from the first main face **12** to the second main face **14** and through at least one of the plurality of polymer stripes **16**. The division line may, e.g., run perpendicular to the first main face **12** and the second main face **14** of the semiconductor wafer **10**. Further, the division line may run along the stripe **16**, i.e., the division line may extend between the side flanges of the stripe **16** and may, e.g., correspond to the central axis of the stripe **16**.

As the thickness of semiconductor wafer **10** may be greater in the second region **32** than in the first region **30** comprising the active structure thereof, the electrical resistance in the first region **30** between the first main face **12** and the second main face **14** is reduced. Thus, due to selective thinning, less heat may be generated inside the semiconductor chip **24** and the heat generated may be transported away from the semiconductor chip **24** faster than in the case when the electrical resistance is larger and/or the thickness of semiconductor wafer **10** is greater in the first region **30**.

The semiconductor chip **24** may, e.g., be separated by a single cut from the first main face **12** to the second main face **14** of the semiconductor wafer **10**. The semiconductor chip **24** may, e.g., be separated by a step cut from the first main face **12** to the second main face **14** of the semiconductor wafer **10**. The step cut may, e.g., comprise sawing the semiconductor wafer **10** with a first saw blade having a first width to produce grooves (not shown) and subsequently sawing the semiconductor wafer **10** with a second saw blade having a second width which is smaller than the first width to complete the division process. That is, sawing with the second saw blade may, e.g., be done until the second saw blade hits or cuts into the dicing tape **28**. In case the process of dicing before grinding (DBG) has been applied to the semiconductor wafer **10**, the semiconductor wafer **10** may be divided, in particular sawn, by starting from the grooves which have been cut in the first main face **12** using the first saw blade. The width of the second saw blade used for completing the dicing may be smaller than the width of the grooves. Irrespective of performing a single cut or a step cut, the width of the (second) saw blade may be smaller than the width of the polymer stripe **16**.

The semiconductor wafer **10** may, e.g., also be cut through at least one of the plurality of polymer stripes **16** and from the second main face **14** towards the first main face **12** of the semiconductor wafer **10**. In this case the semiconductor wafer **10** may, e.g., be placed on the dicing tape **28** with the first main face **12** facing the dicing tape **28**.

By dividing the semiconductor wafer **10** through at least one of the plurality of polymer stripes **16**, this polymer stripe **16** is split up into two polymer structures **17** wherein one polymer structure **17** is associated with a first semiconductor device **100** and the other polymer structure **17** is associated with a second semiconductor device **100** adjacent to the first semiconductor device **100**. In FIG. **1**F four semiconductor devices **100** are shown, wherein the two semiconductor devices **100** depicted on the left and on the right hand side of FIG. **1**F are equipped with a polymer structure **17** only at one of their side faces depicted in FIG. **1**F.

As mentioned above, the semiconductor wafer **10** is divided in a direction along at least one of the plurality of polymer stripes **16**. The polymer stripes **16** may thus run along dicing kerfs of the semiconductor wafer **10**. The viscoelastic material of the polymer stripes **16** may lower the tensile stress occurring at the edge of the second main face of the semiconductor chip **24** when dividing the semiconductor wafer **10** compared to the case of dividing a wafer having a continuous, unpatterned backside metallization. Thus, chip crack propagation or chipping as caused by tensile stress at the chip edge may be avoided by protecting the chip cutting edge by the polymer structure **17**.

Further, if the material of the conductive layer **18** is completely removed from the top surfaces of the stripes **16** during planarization, no conductive material (e.g., metal) is cut when dividing the semiconductor wafer **10** into chips **24**. This facilitates the process of chip separation and/or device fabrication. Even if a thin residual layer (not shown) of conductive material (e.g., metal) remains on the top surfaces of the polymer stripes **16** after planarization, the process of chip separation and/or device fabrication may still benefit from the reduced thickness of the conductive layer at the dicing kerfs (and, additionally, from the polymer chip edge protection).

Further, the polymer structures **17** of singulated semiconductor chips **24** may protect the chip edges during subsequent handling such as, e.g., placement of chips on top of a carrier such as, e.g., a lead frame. The patterning of the backside metallization by, e.g., polymer stripes **16** and a process to remove the metal on the polymer stripes **16** enable and improves the ongoing use of conventional dicing methods like, e.g., sawing or laser dicing (e.g., stealth dicing) of wafers.

The semiconductor wafer **10** may, e.g., be divided multiple times along adjacent parallel and/or crossing polymer stripes **16**. By doing this, a semiconductor device **100** is singulated

from the semiconductor wafer **10**. The semiconductor device **100** may, e.g., comprise the conductive layer **18** (e.g., metal layer) as the backside metallization and two polymer structures **17** arranged along two opposite edges at the second main face **14** of the semiconductor chip **24**. In particular, the semiconductor device **100** may comprise the conductive layer **18** as the backside metallization and four polymer structures **17** arranged along all four edges at the second main face **14** of the semiconductor chip **24**.

The second main face **14** of the semiconductor device **100** may, e.g., be attached on a carrier by gluing, soldering, or sintering. In case the semiconductor device **100** is attached by soldering, a soft solder or a diffusion solder may be used to attach the semiconductor device **100**. The semiconductor chip **24** may, e.g., be attached with the second main face **14** on the carrier. The carrier may, e.g., be one of a lead frame, a ceramics substrate such as, e.g., a DCB (direct copper bonded) ceramics substrate, and a printed circuit board (PCB).

FIGS. **2**A-**2**E schematically illustrate a method of manufacturing a semiconductor device **200** in accordance with one embodiment. This method is similar to the method described in the FIGS. **1**A-**1**F; however it comprises forming a base metallization layer **20** on the plurality of polymer stripes **16** and on the second main face **14** of the semiconductor wafer **10**, before the first metallization layer **22** is formed on the base metallization layer **20**.

FIG. **2**A schematically illustrates providing a semiconductor wafer **10** having a first main face **12** and a second main face **14** wherein the second main face **14** is the backside of the semiconductor wafer **10**. The semiconductor wafer **10** which is depicted in FIG. **2**A has the same features as the semiconductor wafer **10** of FIG. **1**A. In particular this applies to the dimensions of the semiconductor wafer **10**, and the two (optional) steps of dicing before grinding and thinning the semiconductor wafer **10**.

In FIG. **2**B, a plurality of polymer stripes **16** is formed on the second main face **14** of the semiconductor wafer **10**. The polymer stripes **16** of FIG. **2**B have the same features as the polymer stripes **16** of FIG. **1**B. In particular this applies to the material and the dimensions of the polymer stripes **16** and the method of forming the polymer stripes **16** on the semiconductor wafer **10**. Further, FIG. **2**B illustrates removing wafer material at the exposed second main face **14** of the semiconductor wafer **10**. The step of selectively removing wafer material has the same features as the step which is described in FIG. **1**C. In particular this applies to the method of removing the wafer material at the exposed second main face **14** of the semiconductor wafer **10** and the location where the wafer material is removed at the semiconductor wafer **10**. The semiconductor wafer **10** after the step of removing wafer material has the same features as the semiconductor wafer **10** of FIG. **1**C.

FIGS. **2**B and **2**C illustrate forming an electrically conductive layer **18** on the plurality of polymer stripes **16** and on the second main face **14** of the semiconductor wafer **10**. The conductive layer **18** may comprise or consist of a base metallization layer **20** and the first metallization layer **22**. FIG. **2**B illustrates forming a base metallization layer **20** on the plurality of polymer stripes **16** and on the second main face **14** of the semiconductor wafer **10**. FIG. **2**C illustrates forming the first metallization layer **22** on the base metallization layer **20**.

The base metallization layer **20** may, e.g., be formed using at least one of sputtering, CVD, PVD, electroplating, electroless plating, and spray plating. A material of the base metallization layer **20** may, e.g., be at least one of Au, Al, Ti, W, Cr, NiCo, Co, Cu, Sn, Ni, NiV, NiSn, Au, Ag, Pt, Pd, and an alloy of one or more of these metals.

The base metallization layer **20** of FIG. **2**B may be a multi-layer structure (not shown). By way of example, the base metallization layer **20** may be manufactured by sputtering first a layer of Al, then a layer of Ti on the Al layer, and finally a layer of NiV on top of the Ti layer. The thickness of the Al layer may be about 200 nm, the thickness of the Ti layer may be about 400 nm and the thickness of the Ti layer may be about 200 nm. The total thickness H**3** of the base metallization layer **20** may be between 50 and 2000 nm, in particular between 200 and 1000 nm.

After forming the base metallization layer **20** on the plurality of polymer stripes **16** and on the second main face **14** of the semiconductor wafer **10**, the plurality of polymer stripes **16** may, e.g., be completely covered by the base metallization layer **20**. More specifically, the base metallization layer **20** may be unstructured and may, e.g., completely cover the semiconductor wafer **10**.

FIG. **2**C illustrates forming the first metallization layer **22** on the base metallization layer **20**. The first metallization layer **22** of FIG. **2**C may have the same features and may be applied the same way as the first metallization layer **22** of FIGS. **1**D-**1**F.

The first metallization layer **22** may be formed by depositing, e.g., sputtering, plating etc., a metal layer having a thickness H**5**. H**5** may, e.g., be greater than 5, 10, 15, 20, 25, 30, 50 μm and may thus be in the same range as the thickness H**1** of the first metallization layer **22** in FIGS. **1**D-**1**F. Similar to FIGS. **1**D-**1**F, the total thickness of the conductive layer **18** in FIGS. **2**C-**2**D is denoted by H**1** in regions between adjacent polymer stripes **16** and H**1'** in regions on top of the polymer stripes **16**. Here, H**1** may equal the sum of the thickness H**4** of the base metallization layer **20** and the thickness H**5** of the first metallization layer **22**. The values of H**1** and H**1'** may, e.g., be the same as mentioned before or slightly greater due to the additional thickness H**4** of the base metallization layer **20**.

The first metallization layer **22** which is depicted in FIG. **2**C may have the same features as the first metallization layer **22** of FIG. **1**D. In particular this applies to the first metal material of the first metallization layer **22** and the method of forming the first metallization layer **22**.

After the conductive layer **18** has been formed, the conductive layer **18** and the plurality of polymer stripes **16** may, e.g., be identical in thickness, the conductive layer **18** may, e.g., have a thickness H**1** smaller than the thickness H of the plurality of polymer stripes **16** or the conductive layer **18** may, e.g., have a thickness H**1** greater than the thickness H of the plurality of polymer stripes **16**.

FIG. **2**D illustrates planarizing the conductive layer **18** which comprises the base metallization layer **20** and the first metallization layer **22**. The method shown in FIG. **2**D may comprise the same features as the method shown in FIG. **1**E. This applies in particular to the method for planarizing the conductive layer **18**, the dimensions of the conductive layer **18** and the dimensions of plurality of polymer stripes **16**. This implies that in FIG. **2**D, planarizing the conductive layer **18** may cause structuring both the base metallization layer **20** and the first metallization layer **22**. Thus, the exposed surfaces of the plurality of polymer stripes **16** and the exposed upper surfaces of the structured conductive layer **18** may again completely cover the second main face **14** of the semiconductor wafer **10**. Here, each of the exposed upper surfaces of the structured conductive layer **18** may be composed of an

inner surface area provided by the first metallization layer **22** and an outer surface area provided by the base metallization layer **20**.

FIG. **2**E illustrates dividing the semiconductor wafer **10** in semiconductor chips **24** in order to produce semiconductor devices **200**. The method shown in FIG. **2**E may comprise the same features as the method shown in FIG. **1**E. This applies in particular to the method of dividing, the location and orientation of the division line, and the method of attaching the semiconductor chip **24** on a carrier.

FIGS. **3**A-**3**E schematically illustrate a method of manufacturing a semiconductor device **300** in accordance with one embodiment. This method is similar to the methods described in the FIGS. **1**A-**1**F and **2**A-**2**E; however it comprises forming a bonding layer **26**, e.g., a second metallization layer, on top of the first metallization layer **22**. This bonding layer **26** may, e.g., comprise or consist of a bonding material, e.g., a solder material comprising Sn and/or other metals used for soldering.

FIG. **3**A corresponds to FIGS. **1**A and **2**A and reference is made to the corresponding disclosure.

In FIG. **3**B, a plurality of polymer stripes **16** is formed on the second main face **14** of the semiconductor wafer **10**. The plurality of polymer stripes **16** of FIG. **3**B has the same features as the plurality of polymer stripes **16** of FIG. **1**B or FIG. **2**B. In particular this applies to the material and the dimensions of the polymer stripes **16** and the method of forming the polymer stripes **16** and on the semiconductor wafer **10**.

Further, FIG. **3**B illustrates removing wafer material at the exposed second main face **14** of the semiconductor wafer **10**. The step of removing the material has the same features as the steps described in FIGS. **1**C or **2**B. In particular this applies to the method of removing the wafer material at the exposed second main face **14** of the semiconductor wafer **10** and the location where the wafer material is removed at the semiconductor wafer **10**. The semiconductor wafer **10** after the step of removing wafer material has the same features as the semiconductor wafer **10** of FIG. **1**C or **2**B.

FIGS. **3**B and **3**C illustrate forming a conductive layer **18** on the plurality of polymer stripes **16** and on the second main face **14** of the semiconductor wafer **10**. FIG. **3**B illustrates forming a base metallization layer **20** on the plurality of polymer stripes **16** and on the second main face **14** of the semiconductor wafer **10** as described in conjunction with FIG. **2**B.

FIG. **3**C illustrates forming a first metallization layer **22** on the base metallization layer **20** and forming a bonding layer **26** on the first metallization layer **22**. The first metallization layer **22** which is depicted in FIG. **3**C has the same features as the first metallization layer **22** of FIGS. **1**D or **2**C. In particular this applies to the material of the first metallization layer **22**, the dimensions, and the method of forming the first metallization layer **22**.

After forming the first metallization layer **22**, the bonding layer **26** is formed on the first metallization layer **22**. The thickness of the bonding layer **26** is H**6**. The thickness H**1** of the conductive layer **18** is the sum of the thickness H**4** of the base metallization layer **20**, the thickness H**5** of the first metallization layer **22** and the thickness H**6** of the bonding layer **26**. H**5** may have the same dimensions as mentioned above. H**6** may be smaller than H**5**. By way of example, H**6** may, e.g., be smaller than 3, 5 or 10 μm.

The bonding layer **26** may consist of or comprise a second metal material. The second metal material may be a solder material, e.g., be Sn. In a specific example, the thickness H**5** of the first metallization layer **22** and the thickness H**6** of the bonding layer **26** are, e.g., about 5 μm and 3 μm, respectively. Both the first metallization layer **22** and the bonding layer **26** may be applied by a deposition method as mentioned above, e.g., by sputtering or plating. The bonding layer **26** may be used as a bonding material (e.g., solder) deposit after the semiconductor device **300** has been finished.

FIG. **3**D illustrates planarizing the conductive layer **18** which comprises the base metallization layer **20**, the first metallization layer **22** and the bonding layer **26**. The method shown in FIG. **3**D may comprise the same features as the method shown in FIGS. **2**D and **1**E. This applies in particular to the method of planarizing the conductive layer **18**. By planarization, the bonding layer **26** may be structured into bond material deposits, e.g., solder deposits.

FIG. **3**E illustrates dividing the semiconductor wafer **10** into single chips **24**. The method shown in FIG. **3**E comprises the same features as the method shown in FIG. **1**F or **2**E. This applies in particular to the method of dividing and the location and orientation of the division line.

The semiconductor devices **300** manufactured that way may be attached to a carrier by using the bond material of bonding layer **26**. In particular, the bond material may be a bond material configured to establish diffusion solder bonds. By way of example, the bond material may comprise one or more of Sn, SnAg, SnAu, SnCu, In, InAg, InCu and InAu. The semiconductor devices **300** may be bonded to a carrier without the need to apply additional solder material, i.e., without the need to perform an additional solder deposit attach step before device mounting.

FIGS. **4**A-**4**E schematically illustrate a method of manufacturing a semiconductor device **400** in accordance with one embodiment. This method is similar to the methods described in the FIGS. **1**A-**1**F, **2**A-**2**E and **3**A-**3**E. However, compared to the embodiment of FIGS. **1**A-**1**F, the conductive layer **18** comprises or is a metal paste layer **22'**. The metal paste layer **22'** may be formed by a technique such as, e.g., by scraping, squeegeeing, printing, dispensing, etc.

FIG. **4**A corresponds to FIGS. **1**A, **2**A, **3**A and reference is made to the corresponding disclosure.

In FIG. **4**B, a plurality of polymer stripes **16** is formed on the second main face **14** of the semiconductor wafer **10**. The plurality of polymer stripes **16** of FIG. **4**B has the same features as the plurality of polymer stripes **16** of FIGS. **1**B, **2**B and **3**B. In particular this applies to the material and the dimensions of the polymer stripes **16** and the method of forming the polymer stripes **16** and on the semiconductor wafer **10**.

Further, FIG. **4**B illustrates removing wafer material at the exposed second main face **14** of the semiconductor wafer **10**. The step of removing the material has the same features as the steps described in FIG. **1**C, **2**B or **3**B. In particular this applies to the method of removing the wafer material at the exposed second main face **14** of the semiconductor wafer **10** and the location where the wafer material is removed at the semiconductor wafer **10**. The semiconductor wafer **10** after the step of removing wafer material has the same features as the semiconductor wafer **10** of FIG. **1**C, **2**B or **3**B.

FIG. **4**C illustrates forming a conductive layer **18** on the plurality of polymer stripes **16** and on the second main face **14** of the semiconductor wafer **10**. In the embodiment of FIG. **4**C, the conductive layer **18** may, e.g., comprise or consist of a metal paste layer **22'**. The metal paste layer **22'** of FIG. **4**C may, e.g., comprise or consist of one or more metal paste layers. The metal paste may containing metal particles dispersed within an organic material. The metal paste may, e.g., be a nano paste, a solder paste, in particular a diffusion solder paste, and a conductive adhesive.

The thickness of the metal paste layer **22'** over regions of the second main face **14** which are not covered by a polymer stripe **16** is H**7**. The thickness H**7** may, e.g., be larger than the thickness H of the plurality of polymer stripes **16**. In another case, the thickness H**7** of the metal paste layer **22'** may, e.g., be smaller than the thickness H of the plurality of polymer stripes **16**.

The metal paste layer **22'** of FIG. **4**C may be applied by scraping, squeegeeing, printing, laminating, in particular laminating using a prepared foil, dispensing, spin-coating, or combination of these techniques. After forming the metal paste layer **22'** of FIG. **4**C using the metal paste, the plurality of polymer stripes **16** may, e.g., be completely covered by the metal paste. Further, the metal paste layer **22'** may completely cover the second main face **14** of the semiconductor wafer **10**.

After forming the metal paste layer **22'** of FIG. **4**C, the metal paste layer **22'** may, e.g., be dried. After drying, the metal paste layer **22'** may optionally be hardened. This may, e.g., be carried out by applying heat to the metal paste layer **22'**. By heating the metal paste layer **22'**, the organic material may, e.g., be cured, pre-cured or evaporated. By way of example, the organic material may be a B-stage polymer material.

FIG. **4**D illustrates planarizing the conductive layer **18** which comprises or consists of the metal paste layer **22'**. The method shown in FIG. **4**D may comprise the same features as the methods shown in FIGS. **1**E, **2**D and **3**D. This applies in particular to the method of planarizing the conductive layer **18** or to the method of planarizing the conductive layer **18** and the plurality of polymer stripes **16**. FIG. **4**D shows that after planarizing the conductive layer **18** (e.g., the metal paste layer **22'**) and the plurality of polymer stripes **16**, the plurality of polymer stripes **16** may be exposed and the conductive layer **18** may be structured. However, as explained earlier, it may also be the case that a thin residual metal paste layer still covers the top of the polymer stripes **16**.

The thickness H**2** of the (e.g., structured) conductive layer **18** after planarization is greater than the thickness H**3** of the plurality of polymer stripes **16**. It is to be noted that H**3** may be smaller than H, i.e., that the exposed surfaces of the polymer stripes **16** in FIG. **4**D are surfaces created by planarization. It is also to be noted that H**2** may be smaller than H**7**, i.e., that the conductive layer **18** in regions between adjacent polymer stripes **16** has been thinned by the planarization of FIG. **4**D.

FIG. **4**E illustrates dividing the semiconductor wafer **10** into single chips **24** to produce semiconductor devices **400**. The method shown in FIG. **4**E may comprise the same features as the method shown in FIGS. **1**F, **2**E and **3**E. This applies in particular to the method of dividing and the location and orientation of the division line.

The individual semiconductor devices **400** may then be attached to a carrier (e.g., lead frame). In some cases, the structured metal paste layer **22'** may be used as a bonding material. In these cases, no additional bonding material may be necessary.

FIGS. **5**A-**5**E schematically illustrate a method of manufacturing a semiconductor device **500** in accordance with one embodiment. This method is similar to the methods described in the FIGS. **1**A-**1**F, **2**A-**2**E, **3**A-**3**E and **4**A-**4**E. However, compared to the embodiment of FIGS. **4**A-**4**E, a base metallization layer **20** is applied on the plurality of polymer stripes **16** and on the second main face **14** of the semiconductor wafer **10** before applying the metal paste layer **22'**.

FIG. **5**A corresponds to FIGS. **1**A, **2**A, **3**A and **4**A and reference is made to the corresponding disclosure.

In FIG. **5**B, a plurality of polymer stripes **16** is formed on the second main face **14** of the semiconductor wafer **10**. The plurality of polymer stripes **16** of FIG. **5**B has the same features as the plurality of polymer stripes **16** of FIGS. **1**B, **2**B, **3**B and **4**B. In particular this applies to the material and the dimensions of the polymer stripes **16** and the method of forming the polymer stripes **16** and on the semiconductor wafer **10**.

Further, FIG. **5**B illustrates removing wafer material at the exposed second main face **14** of the semiconductor wafer **10**. The step of removing the material has the same features as the steps described in FIG. **1**C, **2**B, **3**B or **4**B. In particular this applies to the method of removing the wafer material at the exposed second main face **14** of the semiconductor wafer **10** and the location where the wafer material is removed at the semiconductor wafer **10**. The semiconductor wafer **10** after the step of removing wafer material has the same features as the semiconductor wafer **10** of FIG. **1**C, **2**B, **3**B or **4**B.

FIGS. **5**B and **5**C illustrate forming a conductive layer **18** on the plurality of polymer stripes **16** and on the second main face **14** of the semiconductor wafer **10**. FIG. **5**B illustrates forming the base metallization layer **20** on the plurality of polymer stripes **16** and on the second main face **14** of the semiconductor wafer **10**. The method of forming the base metallization layer **20** may comprise the same features as the method shown in FIG. **2**B or FIG. **3**B. This applies in particular to the material and dimensions of the base metallization layer **20** and the method of forming the base metallization layer **20**.

FIG. **5**C illustrates forming the metal paste layer **22'** on the base metallization layer **20**. The metal paste layer **22'** of FIG. **5**C may have the same features as the metal paste layer **22'** of FIG. **4**C. In particular this applies to the material(s) of the metal paste layer **22'** and the method of forming the metal paste layer **22'**. The thickness H**8** of the conductive layer **18** is the sum of the thickness H**7** of the metal paste layer **22'** and the thickness H**4** of the base metallization layer **20**. The thickness H**8** of the conductive layer **18** may, e.g., be greater than the thickness H of the plurality of polymer stripes **16**. However in another case, the thickness H**8** of the conductive layer **18** may, e.g., be smaller than the thickness H of the plurality of polymer stripes **16**. The thickness H**8** may be in the same range as the thickness H**7** of FIG. **4**C.

After forming the metal paste layer **22'** of FIG. **5**C, the same steps as mentioned above may be used, e.g., to dry and/or harden the metal paste layer **22'**.

FIG. **5**D illustrates planarizing the conductive layer **18** which comprises the base metallization layer **20** and the metal paste layer **22'**. The method shown in FIG. **5**D may comprise the same features as the method shown in FIGS. **1**E, **2**D, **3**D and **4**D.

FIG. **5**E illustrates dividing the semiconductor wafer **10** into single chips **24** to produce semiconductor devices **500**. The method shown in FIG. **5**E may comprise the same features as the method shown in FIGS. **1**F, **2**E, **3**E and **4**E. This applies in particular to the method of dividing, the location and orientation of the division line, and the method of attaching the semiconductor chip **24** on a carrier.

FIG. **6** schematically illustrates a cross-section of semiconductor devices **100** and **400**. The semiconductor device **100**, **400** comprises a semiconductor chip **24** having a first main face **12** and a second main face **14**.

The semiconductor chip **24** may, e.g., be a logic integrated circuit and the conductive layer **18** may, e.g., be a backside heat sink. The backside heat sink may not be electrically coupled to the logic integrated circuit, i.e., may not constitute a chip electrode. In other cases, the conductive layer **18** may

be electrically coupled to the logic integrated circuit by through vias running through the chip.

The semiconductor chip **24** may, e.g., be a power semiconductor chip having a backside electrode **40** at the second main face **14**. The backside electrode **40** is electrically connected to the active structure implemented in the semiconductor chip **24**. By way of example, the backside electrode **40** may be an electrode of a power semiconductor chip **24**. The backside electrode **40** may, e.g., be the drain electrode of a MOSFET or a JFET, the collector electrode of an IGBT or a bipolar transistor or the anode of a diode. During operation, voltages higher than 5, 50, 100, 500 or even 1000 V may be applied between the backside electrode **40** and a front side electrode (not shown) of such power semiconductor chip **24**.

The semiconductor device **100**, **400** may, e.g., comprise a structured conductive layer **18** which is arranged on a first region **30** of the second main face **14** of the semiconductor chip **24**. One should note that the second main face **14** of the semiconductor chip **24** is not flat but has an elevated second region **32** such as, e.g., an elevated rim. The first main face **12** of the semiconductor chip **24** may, e.g., be essentially flat. The conductive layer **18** may, e.g., be coupled to the drain electrode **40** of a power transistor or an anode of a power diode. Still further, the semiconductor device **100**, **400** may, e.g., comprise a polymer structure **17** on a second region **32** of the second main face **14** of the semiconductor chip **24**, see FIGS. **9** and **10**. The second region **32** is a peripheral region of the second main face **14** of the semiconductor chip **24** and the level of the first region **30** and the level of the second region **32** are different. Between the first region **30** and the second region **32** may, e.g., extend an intermediate region **31** of the second main face **14**, wherein the level of the intermediate region **31** changes from the first region **30** towards the second region **32**. The slope of the intermediate region **31** may, e.g., be different or the same as the slope of the flanges of the polymer structure **17**. The area of the second main face **14** may, e.g., be the sum of the area of the first region **30**, the second region **32** and the intermediate region **31**.

The first region **30** may, e.g., have a rectangular or quadratic shape. The intermediate region **31** may, e.g., have a shape of a closed frame which surrounds the shape of the first region **30**, wherein the individual sides of the frame are inclined as compared to the level of the first region **30** and the level of the second region **32**. The second region **32** may, e.g., have a shape of a closed frame which surrounds the outline of the intermediate region **31** and the first region **30**.

The thickness D**1** of the semiconductor chip **24** corresponds to the thickness T**1** of the wafer **10** in the second region **32** and may, e.g., be smaller than 100 μm, in particular smaller than 60 μm, and more in particular smaller than 40 μm or even 30 μm. The thickness D**3** of the semiconductor chip in the first region **30** may, e.g., be smaller than 50 μm, in particular smaller than 30 μm, and more in particular smaller than 20 μm or even 15 μm.

A lateral face **34** of the polymer structure **17** may, e.g., be flush with a lateral face **36** of the semiconductor chip **24**, see e.g., FIGS. **6-8**. This means that the lateral face **34** of the polymer structure **17** lies in the same plane as the lateral face **36** of the semiconductor chip **24**. The lateral faces **34** and **36** lie on the same side of the semiconductor device **100**, **400**. That is, a common lateral face **34**, **36** of the semiconductor chip **24** and the polymer structure **17** may be generated when the semiconductor wafer **10** comprising the polymer stripes **16** on the second main face **14** is singulated into single semiconductor chips **24** or semiconductor devices **100**, **400** as described before in conjunction with FIGS. **1**F and **4**E.

The polymer structure **17** may, e.g., comprise or consist of an imide, in particular a photoimide, a photoresist, a thermosetting material or a thermoplastic material. The polymer structure **17** may, e.g., have a thickness D**2** corresponding to the thickness H**2** between 3 and 20 μm, in particular between 9 and 15 μm, and a width W between 2 and 50 μm, in particular between 5 and 30 μm. The width W of the polymer structure **17** may, e.g., decrease from the second main face **14** in a direction away from the semiconductor chip **24**. The width W of the polymer structure **17** may, e.g., also be constant from the second main face **14** in a direction away from the semiconductor chip **24**.

The conductive layer **18** of FIG. **6** may, e.g., comprise or consist of the first metallization layer **22** of the first metal as used for semiconductor device **100**. In this case, the semiconductor device **100** of FIG. **6** may, e.g., be manufactured by the method shown in FIGS. **1**A-**1**F.

The conductive layer **18** of FIG. **6** may, e.g., comprise or consist of the metal paste layer **22'** of a metal paste as used for semiconductor device **400**. In this case, the semiconductor device **400** of FIG. **6** may, e.g., be manufactured by the method shown in FIGS. **4**A-**4**E.

The conductive layer **18** may, e.g., have a thickness between 0.5 and 50 μm or 0.5 and 25 μm, in particular between 1 and 10 μm, more in particular between 2 and 7 μm. Further, the thickness of the conductive layer **18** may be greater than 1, 3, 10, 15, 20, 25 or 50 μm.

A surface of the polymer structure **17** facing away from the semiconductor chip **24** and a surface of the conductive layer **18** facing away from the semiconductor chip **24** may, e.g., lie in the same plane as shown in FIG. **6**. The thickness of the conductive layer **18** may, e.g., be larger than the thickness D**2** of the polymer structure **17**, as shown in FIG. **6**. The lateral face **36** of the semiconductor chip **24** may, e.g., have a recess **38** in an upper region of the lateral face **36**. The reason for this recess **38** may, e.g., be a step cut caused by partially sawing the semiconductor wafer **10** using a saw blade of greater width and then completing the singulation by using a saw blade of smaller width.

FIG. **7** schematically illustrates a cross-section of semiconductor devices **200** and **500**. The semiconductor devices **200**, **500** of FIG. **7** are similar to the semiconductor devices **100**, **400** of FIG. **6**, and reference is made to the above disclosure to avoid reiteration; however the conductive layer **18** has a different composition.

The semiconductor chip **24** of FIG. **7** comprises the same features as the semiconductor chip **24** of FIG. **6**. This applies in particular to the type, dimensions, orientation, arrangement and components. The polymer structure **17** of the semiconductor device **100** of FIG. **7** comprises the same features as the polymer structure **17** of the semiconductor device **100** of FIG. **6**. This applies in particular to the dimensions, orientation and arrangement. The arrangement of the semiconductor chip **24** and the polymer structure **17** with the respect to the conductive layer **18** in FIG. **7** shows the same features as the arrangement of these components in FIG. **6**.

The conductive layer **18** of FIG. **7** according to semiconductor device **200** (or semiconductor device **500**) may, e.g., comprise a base metallization layer **20** and a first metallization layer **22** (or metal paste layer **22'**), wherein the base metallization layer **20** is arranged between the polymer structure **17** and the second main face **14** of the semiconductor chip **24** at one side and the first metallization layer **22** (or metal paste layer **22'**) at the other side. The first metallization layer **22** comprises the same features as the first metallization layer **22** of FIG. **6** and the metal paste layer **22'** comprises the same features as the metal paste layer **22'** of FIG. **6**. This applies in

particular to the dimensions, orientation, arrangement and components. The base metallization layer **20** may, e.g., have a thickness between 50 and 2000 nm, in particular between 200 and 1000 nm.

The semiconductor device **200** of FIG. **7** may be manufactured by the method exemplified in FIGS. **2**A-**2**E and the semiconductor device **500** of FIG. **7** may be manufactured by the method exemplified in FIGS. **5**A-**5**E. Reference is made to the corresponding description to avoid reiteration.

FIG. **8** schematically illustrates a cross-section of a semiconductor device **300**. The semiconductor device **300** of FIG. **8** is similar to the semiconductor devices **100** of FIGS. **6** and **200** of FIG. **7**; however the conductive layer **18** has a different composition. Compared to the semiconductor devices **100**, **200**, the semiconductor device **300** of FIG. **8** further comprises a bonding layer **26**.

As to the components of semiconductor device **300** which have already been described in the context of semiconductor devices **100** or **200**, reference is made to the corresponding disclosure. The conductive layer **18** of FIG. **8** may, e.g., comprise the bonding layer **26** of a second material. The bonding layer **26** may, e.g., cover the first metallization layer **22**. The second material may, e.g., be a bonding material such as, e.g., a solder material or a conductive adhesive. The semiconductor device **300** of FIG. **8** may, e.g., be manufactured by the method shown in FIGS. **3**A-**3**E.

Semiconductor devices **100** to **500** are merely examples and several modifications of these exemplary devices **100** to **500** and combinations of specific features exemplified by devices **100** to **500** are possible. By way of example, the semiconductor device **300** as illustrated in FIG. **8** may also be designed without having a base metallization layer **20** similar to semiconductor devices **100**, **400**. In this case, the conductive layer **18** of semiconductor device **300** has a first metallization layer **22** and a bonding layer **26**. Further, the semiconductor devices **400**, **500** using a metal paste layer **22'** may also be equipped with an additional bond material layer similar to the bonding layer **26** of FIG. **8**.

FIG. **9** schematically illustrates a bottom view (footprint) of the semiconductor devices **100** to **500** in accordance with one embodiment. FIG. **9** shows the planarized surfaces of the conductive layer **18** and of the polymer structure **17**. The first region **30** is defined as the region of the second main face **14** of the semiconductor chip **24** where the conductive layer **18** is arranged. The second region **32** is defined as the region of the second main face **14** of the semiconductor chip **24** where the polymer structure **17** is arranged. The intermediate region **31** is to find as the region of the second main face **14** between the first region **30** and the second region **32**.

The second region **32** may, e.g., be a peripheral region of the second main face **14** of the semiconductor chip **24** and the first region **30** may, e.g., be in between portions of the second region **32**. The intermediate region **31** is arranged between the first region **30** and the second region **32**. The dashed lines illustrate the separation lines between (portions of) the intermediate region **31** and (portions of) the second region **32**. The dotted lines illustrate the separation lines between the first region **30** and (portions of) the intermediate region **31**.

In FIG. **9**, two portions of the second region **32** running along two opposite edges of the semiconductor chip **24** are shown. As the width of the polymer structure **17** may decrease from the second main face **14** in a direction away from the semiconductor chip **24**, the second region **32** is larger than the area of the polymer structure **17** on the bottom side of the semiconductor device **100** to **500**, as can be seen in FIG. **9**.

The second main face **14** of the semiconductor chip **24** may, e.g., have a rectangular, in particular quadratic shape. The second region **32** may, e.g., have the shape of at least one stripe comprising at least one straight edge of the second main face **14** of the semiconductor chip **24**. In the embodiment of FIG. **9**, the second region **32** comprises two stripes which are arranged parallel to each other on two opposite edges of the second main face **14** of the semiconductor chip **24**. The second region **32** may, e.g., completely cover two opposing edges of the second main face **14** of the semiconductor chip **24**, as shown in the embodiment of FIG. **9**.

The first region **30** lies in the middle of the second main face **14** of the semiconductor chip **24**. The first region **30** may, e.g., have a quadratic or rectangular shape, wherein the latter is shown in the embodiment of FIG. **9**. The intermediate region **31** is arranged between the first region **30** and the second region **32** and in the embodiment of FIG. **9** may, e.g., comprise two parallel stripes in the view of FIG. **9**. In the embodiment of FIG. **9**, each stripe of the intermediate region **31** is inclined with respect to the level of the first region **30** and the level of the second region **32**. The area of the first region **30** may, e.g., be at least 80%, in particular at least 90%, in more particular at least 95% of the area of the second main face **14** of the semiconductor chip **24**.

FIG. **10** schematically illustrates a bottom view (footprint) of the semiconductor devices **100** to **500** in accordance with one embodiment. The embodiment of FIG. **10** is similar to the embodiment of FIG. **9**; however, the design of the first region **30**, the intermediate region **31**, and the second region **32** is different from the embodiment of FIG. **9**. The intermediate region **31** may, e.g., partly or completely surround the first region **30**, wherein the latter case is shown in the embodiment of FIG. **10**. Accordingly the second region **32** may, e.g., partly or completely surround the intermediate region **31**. In FIG. **10**, the first region **30** may, e.g., have a rectangular or quadratic shape which may, e.g., be centered on the second main face **14** of the semiconductor chip **24**, the intermediate region **31** may, e.g., have the shape of a closed frame, wherein each frame side is inclined with respect to the level of the first region **30**, and the second region **32** may, e.g., have a shape of a closed frame with, e.g., a substantially constant width which completely surrounds the first region **30**. Again, the area of the first region **30** may, e.g., be at least 80%, in particular at least 90%, and more in particular at least 95% of the area of the second main face **14** of the semiconductor chip **24**.

FIG. **11** schematically illustrates a bottom view of one embodiment of a semiconductor arrangement. FIG. **11** shows a semiconductor wafer **10** seen from the bottom (i.e., backside). A plurality of polymer stripes **16** is arranged on the semiconductor wafer **10**. The plurality of polymer stripes **16** comprises a first plurality of parallel polymer stripes **16** and a second plurality of parallel polymer stripes **16** wherein each polymer stripe **16** of the first plurality is orthogonal to each polymer stripe **16** of the second plurality. The first plurality and the second plurality of polymer stripes **16** may be arranged equidistantly wherein the distance between adjacent polymer stripes **16** of the first plurality may be different or may be the same as the distance between adjacent polymer stripes **16** of the second plurality. Between the pluralities of polymer stripes **16**, there is at least one semiconductor chip **24** which is to be singulated. The polymer stripes **16** are arranged on second regions **32** of the wafer backside (i.e., the second main face **14** of the wafer **10**). Regions between the polymer stripes **16** are first regions **30** and intermediate regions **31** where the (structured or unstructured) conductive layer **18** (not shown) is arranged. If structured, the conductive layer **18** is split into insular lands (not shown) separated from each other by polymer stripes **16**, see also FIG. **10**. The semiconductor chips **24** are singulated by separating or dividing, in

particular by sawing or laser dicing, e.g., stealth dicing, the semiconductor wafer **10** along the first plurality of polymer stripes **16** and/or along the second plurality of polymer stripes **16** as described above.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the specific embodiments discussed herein. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A semiconductor device, comprising:

a semiconductor chip comprising a first main face and a second main face, wherein

the second main face comprises a first region and a second region, wherein the second region is a peripheral region of the second main face and a level of the first region and a level of the second region are different such that the second region is thicker than the first region, measured from the first main face to the second main face; and

a polymer structure arranged over the second region of the second main face of the semiconductor chip, wherein an outer lateral face of the polymer structure is flush with a lateral face of the semiconductor chip.

2. The semiconductor device of claim **1**, wherein the first main face of the semiconductor chip is essentially flat.

3. The semiconductor device of claim **1**, wherein a thickness of the semiconductor chip in the second region is less than 100 μm.

4. The semiconductor device of claim **1**, wherein a thickness of the semiconductor chip in the first region is less than 50 μm.

5. The semiconductor device of claim **1**, wherein the second region completely surrounds the first region.

6. The semiconductor device of claim **1**, wherein an intermediate region of the second main face is arranged between the first region and the second region, wherein a level of the intermediate region changes from the first region towards the second region.

7. The semiconductor device of claim **1**, wherein the area of the first region is at least 80%, of the total area of the second main face of the semiconductor chip.

8. The semiconductor device of claim **1**, wherein the second region has the shape of at least one stripe comprising at least one straight edge of the second main face of the semiconductor chip.

9. The semiconductor device of claim **1**, wherein the polymer structure comprises an imide selected from the group consisting of a photoimide, a photoresist, a thermosetting material or a thermoplastic material.

10. The semiconductor device of claim **1**, wherein the polymer structure has a thickness between 3 and 50 μm.

11. The semiconductor device of claim **1**, wherein the polymer structure comprises a stripe having a width between 2 and 50 μm.

12. The semiconductor device of claim **1**, wherein a width of the polymer structure decreases from the second main face in a direction away from the semiconductor chip.

13. The semiconductor device of claim **1**, further comprising an electrically conductive layer arranged on the first region of the second main face of the semiconductor chip.

14. The semiconductor device of claim **13**, further comprising a polymer structure arranged on the second region of the second main face of the semiconductor chip, wherein a thickness of the electrically conductive layer is greater than a thickness of the polymer structure.

15. The semiconductor device of claim **13**, further comprising a polymer structure arranged on the second region of the second main face of the semiconductor chip, wherein a surface of the polymer structure facing away from the semiconductor chip and a surface of the electrically conductive layer facing away from the semiconductor chip are level with each other.

16. The semiconductor device of claim **13**, wherein the electrically conductive layer comprises a first metallization layer of a first material, the first material comprising one of Cu or Sn, or an alloy of one or more of these metals.

17. The semiconductor device of claim **16**, wherein the electrically conductive layer further comprises a bonding layer of a second material, the bonding layer covering the first metallization layer, wherein the second material is a solder material or a conductive adhesive.

18. The semiconductor device of claim **13**, wherein the electrically conductive layer comprises a metal paste layer selected from the group consisting of a nano paste layer, a solder paste layer and a conductive adhesive.

19. The semiconductor device of claim **13**, wherein the electrically conductive layer comprises a base metallization layer, the base metallization layer comprising at least one of Au, Al, Ti, W, Cr, NiCo, Co, Cu, Sn, Ni, NiV, NiSn, Au, Ag, Pt, Pd, and an alloy of one or more of these metals.

20. The semiconductor device of claim **13**, wherein the semiconductor chip is a power semiconductor chip and the electrically conductive layer is coupled to an electrode of the power semiconductor chip.

21. The semiconductor device of claim **13**, wherein the semiconductor chip is a logic integrated circuit and the conductive layer is a backside heat sink.

22. The semiconductor device of claim **1**, further comprising:

an electrically conductive layer arranged over the first region of the second main face of the semiconductor chip, wherein the polymer structure has the shape of a closed frame surrounding the electrically conductive layer.

23. A semiconductor device, comprising:

a semiconductor chip comprising a first main face and a second main face, wherein

the second main face is a backside of the semiconductor chip, the second main face comprises a first region and a second region, the second region is a peripheral region of the second main face and a level of the first region and a level of the second region are different; and

a polymer structure arranged on the second region of the second main face of the semiconductor chip, wherein a width of the polymer structure decreases from the second main face in a direction away from the semiconductor chip.

24. The semiconductor device of claim **23**, wherein the second region completely surrounds the first region.

25. The semiconductor device of claim **23**, wherein an intermediate region of the second main face is arranged between the first region and the second region, wherein a level of the intermediate region changes from the first region towards the second region.

26. The semiconductor device of claim **23**, wherein the second region has the shape of at least one stripe comprising at least one straight edge of the second main face of the semiconductor chip.

27. The semiconductor device of claim **23**, wherein the polymer structure comprises an imide selected from the

group consisting of a photoimide, a photoresist, a thermosetting material or a thermoplastic material.

28. The semiconductor device of claim **23**, further comprising an electrically conductive layer arranged on the first region of the second main face of the semiconductor chip.

29. The semiconductor device of claim **28**, further comprising a polymer structure arranged on the second region of the second main face of the semiconductor chip, wherein a thickness of the electrically conductive layer is greater than a thickness of the polymer structure.

30. The semiconductor device of claim **28**, further comprising a polymer structure arranged on the second region of the second main face of the semiconductor chip, wherein a surface of the polymer structure facing away from the semiconductor chip and a surface of the electrically conductive layer facing away from the semiconductor chip are level with each other.

31. The semiconductor device of claim **28**, wherein the electrically conductive layer comprises a first metallization layer of a first material, the first material comprising one of Cu or Sn, or an alloy of one or more of these metals.

32. The semiconductor device of claim **31**, wherein the electrically conductive layer further comprises a bonding layer of a second material, the bonding layer covering the first metallization layer, wherein the second material is a solder material or a conductive adhesive.

33. The semiconductor device of claim **28**, wherein the electrically conductive layer comprises a metal paste layer selected from the group consisting of a nano paste layer, a solder paste layer and a conductive adhesive.

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